NON VOLATILE MEMORY CELL SENSING CIRCUIT, PARTICULARLY FOR LOW POWER SUPPLY VOLTAGES AND HIGH CAPACITIVE LOAD VALUES

Abstract of the Disclosure

A sensing circuit for a memory cell includes a first bias current generator connected between a first voltage reference and a first inner circuit node, and a second reference current generator connected to the first voltage reference. A comparator having a first input terminal is connected to a comparison circuit node that is connected to the second reference current generator, a second input terminal is connected to a circuit node that is connected to the first inner circuit node, and an output terminal forms an output terminal of the sensing circuit. A cascode-configured bias circuit is connected between the inner circuit node and a matching circuit node. The cascode-configured bias circuit is also connected to a second voltage reference. A current/voltage conversion stage is connected to the matching circuit node, to the comparison circuit node, and to a third voltage reference.